WHAT IS CLAIMED IS:

1. A semiconductor memory formed on a semiconductor substrate comprising;

a first memory cell;

a second memory cell;

a first word line coupled to said first and second memory cells and formed in a first conductive layer;

a first pair of bit lines;

a second pair of bit lines;

a first sense amplifier which provides said first pair of bit lines with a pair of complementary signals on the basis of information of said first memory cell and includes a first pair of MOSFETs,

a second sense amplifier which provides said second pair of bit lines with a pair of complementary signals on the basis of information of said second memory cell and includes a second pair of MOSFETS,

a third and fourth MOSFETs connected in series between said first pair of bit lines;

a fifth MOSFET connected between said first pair of bit lines;

a sixth and a seventh MOSFETs connected in series between said second pair of bit lines; and

a eight MOSFET connected between said second pair of bit lines,

wherein said first pair of bit lines crosses each other with a second conductive layer,

wherein said second pair of bit lines crosses each other with said second conductive layer,

wherein said first pair of MOSFETs and said second pair of MOSFETs are formed in a H-shaped active region,

wherein said third, fourth and fifth MOSFETS are formed in a first T-shaped active region,

wherein said sixth, seventh and eight MOSFEts are formed in a second T-shaped active region, and

wherein said first conductive layer is formed between a surface of said semiconductor substrate and said second conductive layer.

2. A semiconductor memory according to claim 1,

wherein said first memory cell has a ninth MOSFET and a first capacitor,

wherein said second memory cell has a tenth MOSFET and a second capacitor,

wherein plates of said first and second capacitors are formed over said first and second pairs of bit lines.

3. A semiconductor memory according to claim 2, wherein said third, fourth, fifth, sixth, seventh and eight MOSFETs have a common gate electrode.

4. A semiconductor memory according to claim 3, further comprising:

a voltage supply line formed third conductive layer,

wherein said second conductive layer is formed between said third conductive layer and said first conductive layer.